



100

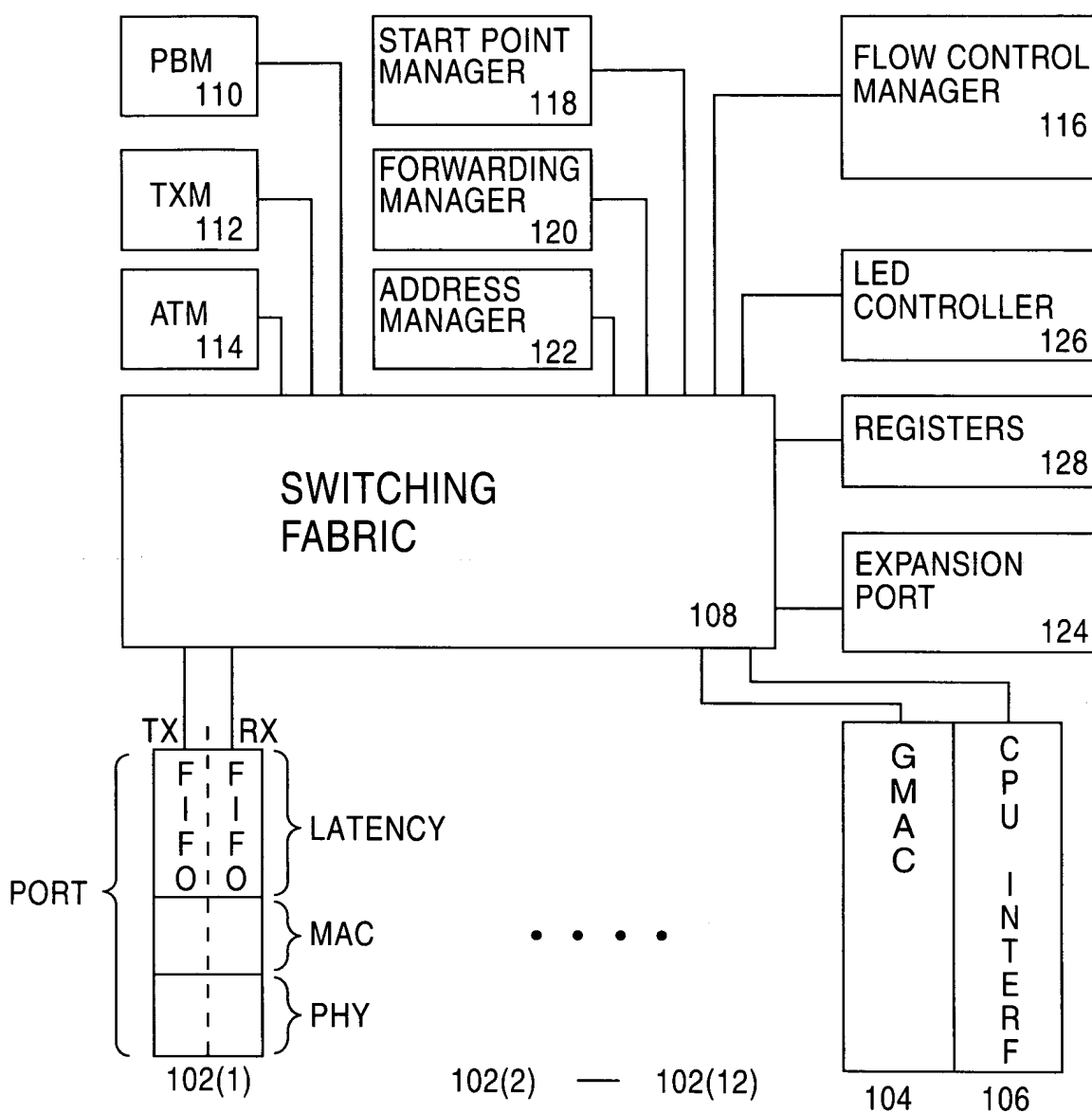


FIG.1A

Figure 1B is a block diagram illustrating a multi-protocol network interface. The diagram shows three memory blocks (PBM 110, ATM 114, TXM 112) connected to three buses (PBM BUS, ATM BUS, TXM BUS). These buses connect to a central processing block containing LATENCY, MAC, and PHY sections. The PBM and TXM sections have a PORT block with four sub-blocks (F, I, F, O). The TXM section also has a TX RX block. The TXM section is connected to an FM 120 block. The TXM section is also connected to an AM 122 block. The TXM section is also connected to an SPM 118 block. The TXM section is also connected to an AM 122 block.

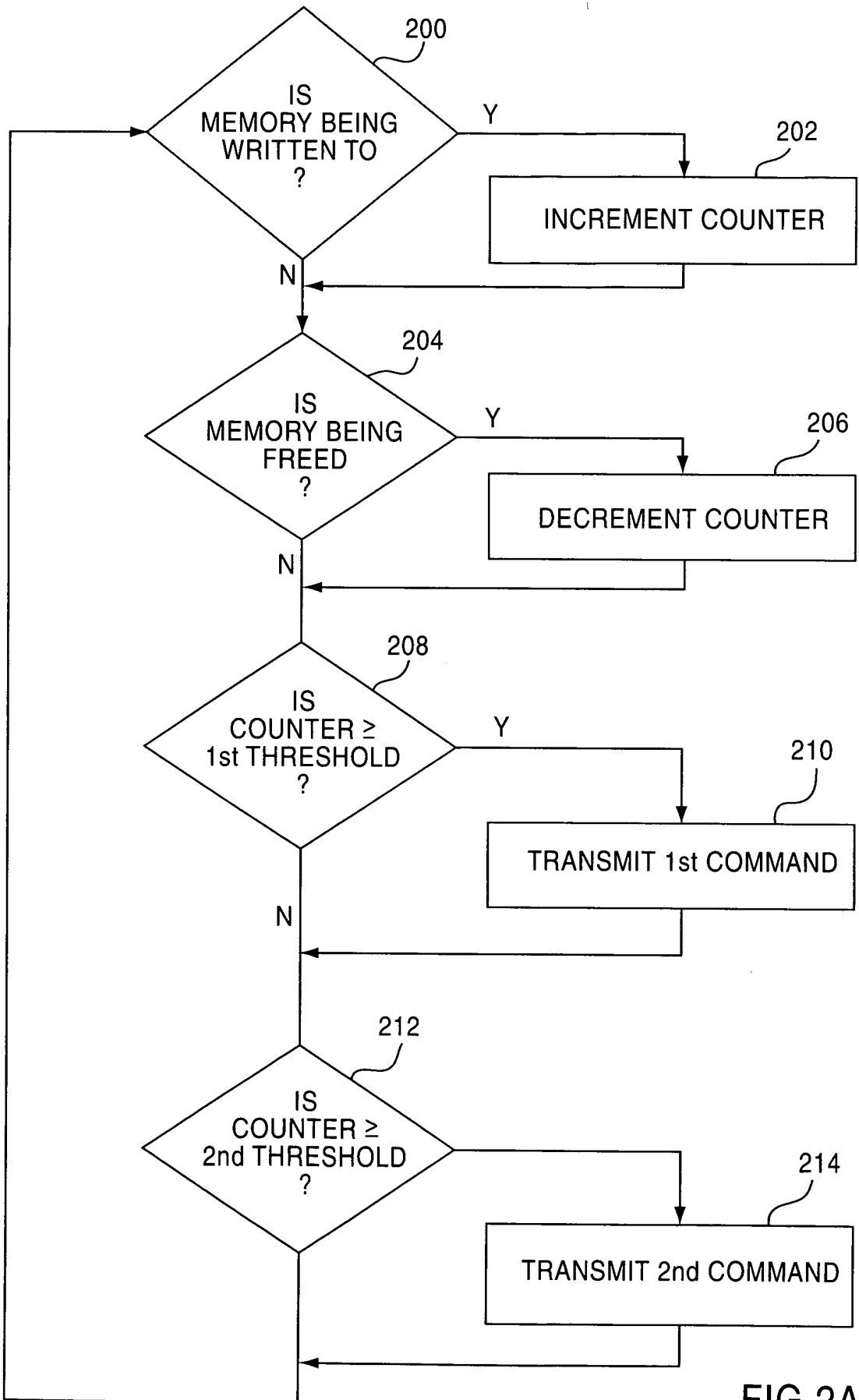


FIG.2A



FCM 116

<div>BUS MONITOR</div> <div>216</div>	<div>COUNTER</div> <div>218</div>
<div>FIRST THRESHOLD COMPARER</div> <div>220</div>	<div>SECOND THRESHOLD COMPARER</div> <div>222</div>

FIG.2B

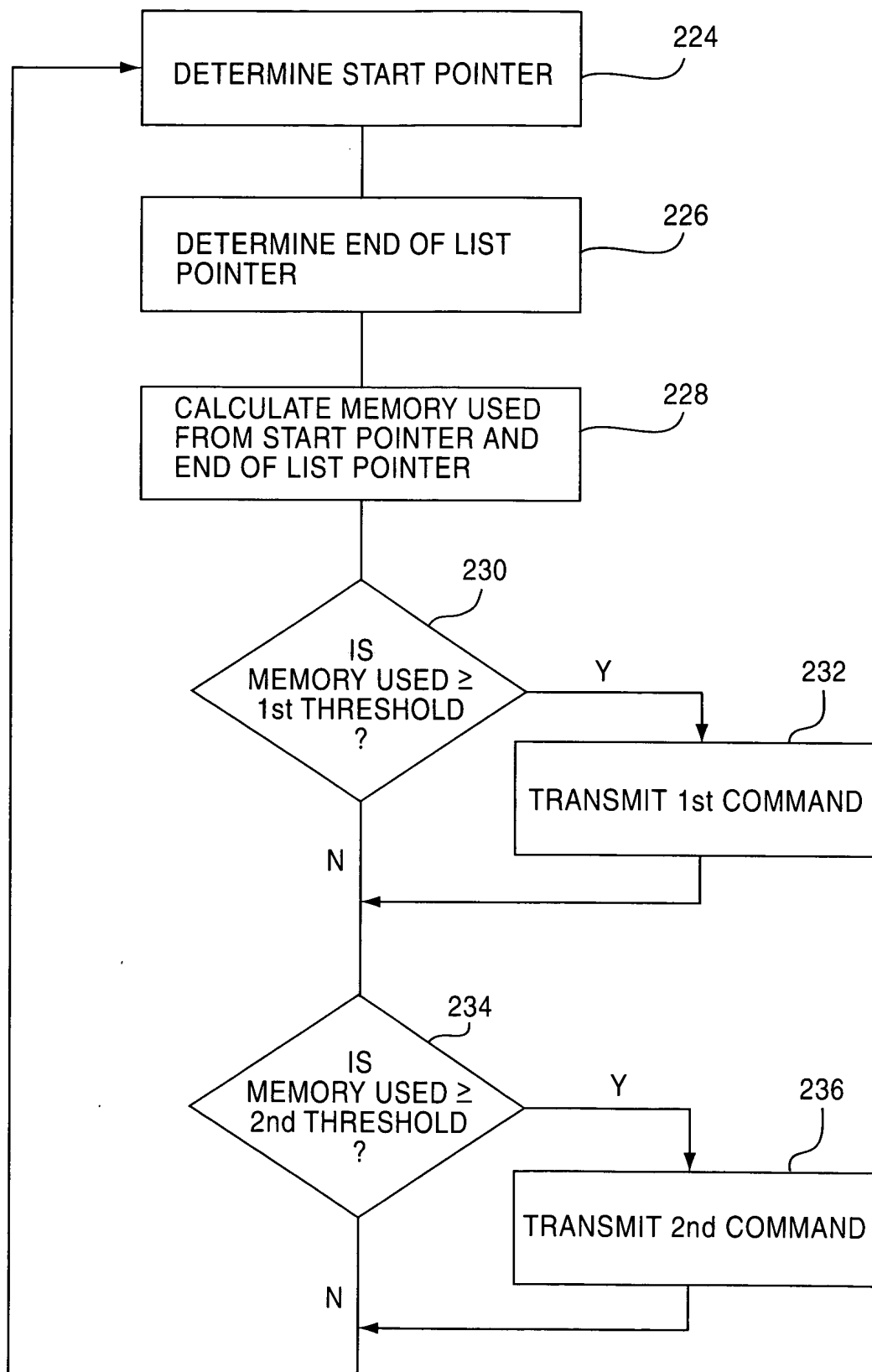


FIG.2C



FCM 116

START POINTER DETERMINER 238	242 MEMORY USED CALCULATOR
END OF LIST POINTER DETERMINER 240	
FIRST THRESHOLD COMPARER 244	246 SECOND THRESHOLD COMPARER

FIG.2D

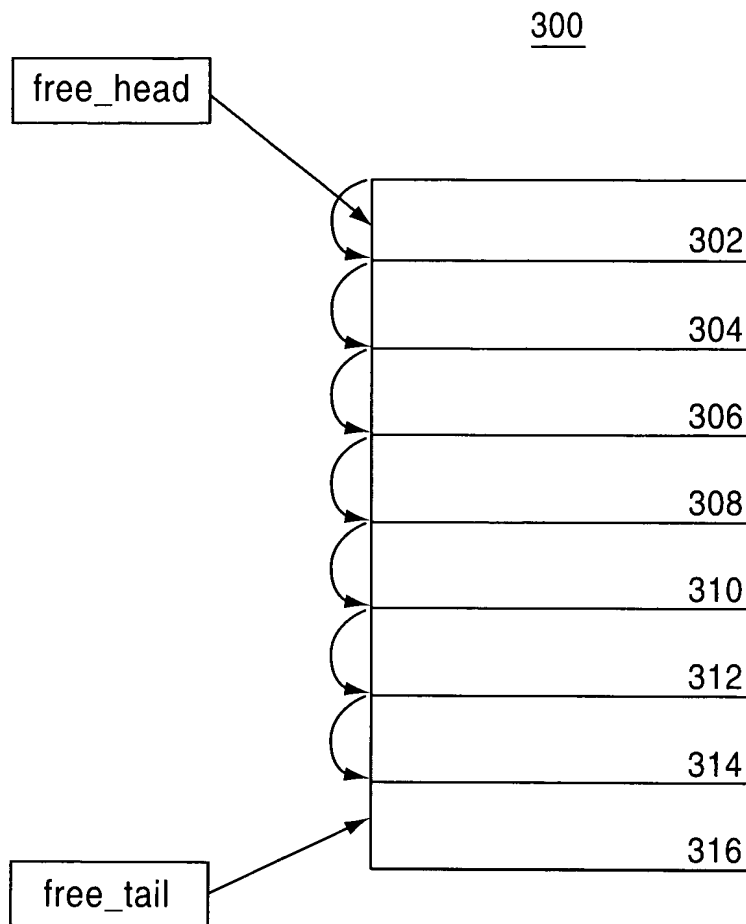


FIG.3A



300

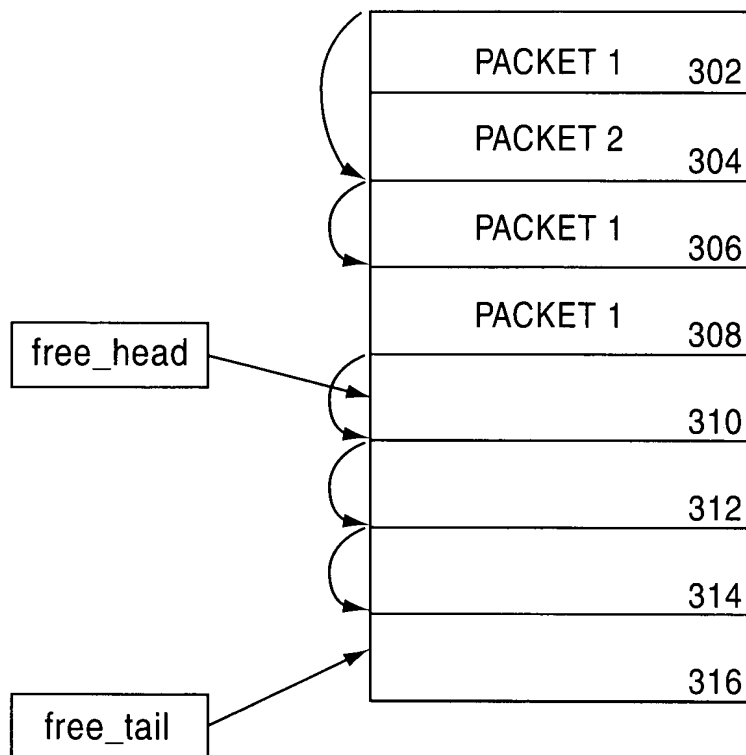


FIG.3B

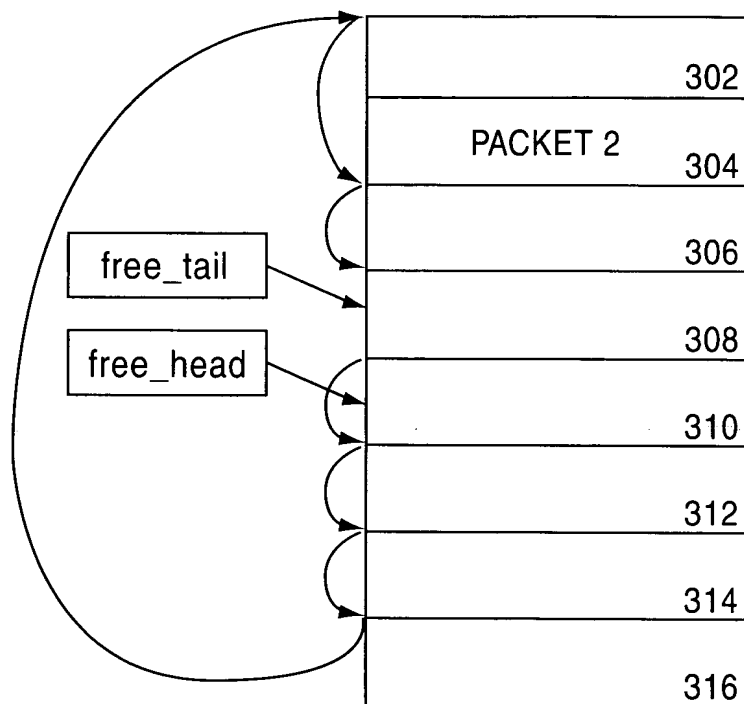


FIG.3C

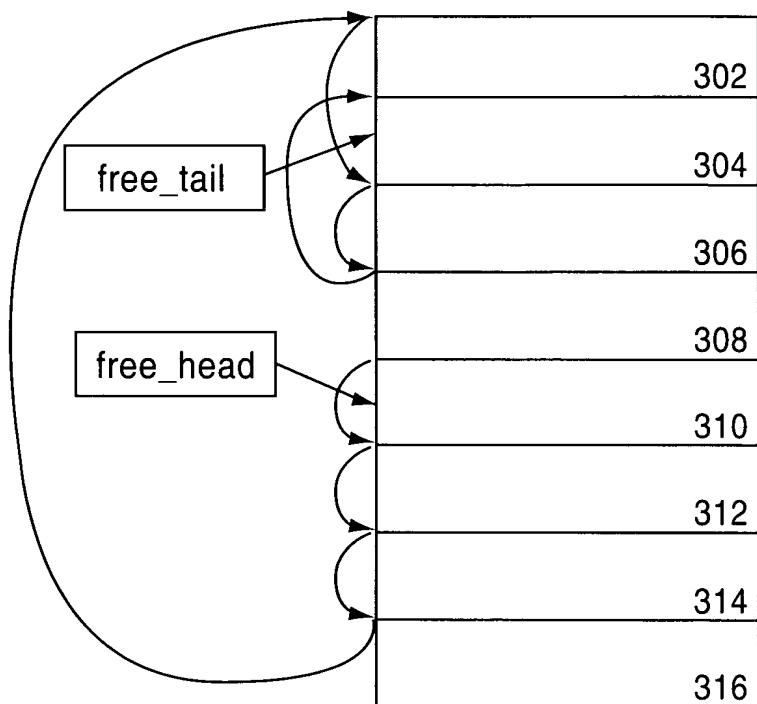


FIG.3D